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Message:

APPLICANT	:	STEPHAN J. JOURDAN et al.
SERIAL NO.	:	09/749,405
FILING DATE	:	December 28, 2000
GROUP ART UNIT	:	2183
FOR	:	METHOD AND APPARATUS FOR PREDICTING BRANCHES USING A META PREDICTOR
EXAMINER	:	Aimee J. Li

PAPER ENTITLED: **REPLY BRIEF** **10 pages**

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Patent

Attorney Docket No.: Intel 2207/7085
Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Commissioner for Patents
P.O. Box 1450
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REPLY BRIEF

Dear Sir:

This Reply Brief is submitted in response to the Examiner's Answer mailed in this case on November 21, 2006.

Appellant submits this Reply Brief to address issues raised in the Examiner's Answer.

REMARKS

Claims 1-8, 10-15, and 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, Hao, and Patt's Alternative Implementations of Hybrid Branch Predictors" (hereinafter "Patt") in view of McFarling's "WRL Technical Note TN-36: Combining Branch Predictors" (hereinafter "McFarling"). Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tran, US Patent 5,822,575, as applied to claim 24, in view of Applicant's admitted prior art.

A. Applicants' reply to Examiner's assertions regarding pages 7-8 of the Appeal Brief. *See* Examiner's Answer, pages 19-20.

The Examiner's position is incorrect and only serves to attempt to muddy otherwise clear waters. As argued previously, there is a fundamental difference between actually *generating* a misprediction value and "factor[ing] into the overall branch prediction scheme" (as the Examiner herself characterizes the role of the cited counter). *See* Examiner's Answer, page 20, line 5. This difference is readily apparent both conceptually and between the present application and the cited art.

Applicants previously argued that the Patt counter is used to keep track of an overall efficiency of a group of predictors. *See* Appeal Brief, page 7. The Examiner, in essence agrees with this assessment, stating the counter "is used to more accurately select which branch predictor to use". *See* Answer, page 20, lines 2-3. That the result of the counter describing overall accuracy may eventually "factor into" the generation of a prediction is not sufficient to support a proper §103(a) rejection. Applicants maintain that this counter is inadequate to describe a meta predictor that itself *generates a misprediction value* as specifically recited in claims of the present application (*see* e.g., claim 1).

B. Applicants' reply to Examiner's assertion regarding page 8-9 and 10 of the Appeal Brief. *See* Examiner's Answer, pages 20-22.

The Examiner asserts that the meaning of the term "misprediction value" is unclear. However, the specification uses the term "misprediction value" in several locations sufficient to clarify that the described misprediction value is different than anything described in the cited references. For example, at page 6, lines 25-26 of the specification, a misprediction value is described as: "Misprediction value 112 then may be used *to decide whether to reverse the prediction provided by the base predictor*, or branch prediction 108." The Examiner latches onto the fact that the section includes the word "may" to state that the definition is not definite. This is improper, as this one section was only isolated for exemplary purposes.

When determining whether a claim term is definite, the claim term is to be read in light of the specification. Though to the Examiner, the term "misprediction value" is unclear standing alone, when read in light of the specification, there is ample description to provide a clear definition for this term. See MPEP 608.01(o); 37 C.F.R. 1.75; and Allen Archery Inc. v. Browning Mfg.Co., 2 U.S.P.Q.2d 1490, 1494 (Fed. Cir. 1987). For example, page 8, lines 15-21 of the specification specifically, definitively describes the relationship of the misprediction value to the reversal of a branch prediction. This section states:

> Misprediction value 112 is used to augment branch prediction 108. Logic gate 214 receives misprediction value 112 and branch prediction 108. Logic gate 214 determines whether to reverse branch 108 according to misprediction value 112. *If misprediction value 112 predicts that branch prediction is correct, then logic gate 214 does not reverse branch prediction 108. If misprediction value 112 predicts that branch prediction is incorrect, then logic gate 214 reverses branch prediction 108.* Using the inputs, logic gate 214 generates a final prediction 216. Final prediction 216 predicts whether the branch instruction should be taken or not taken. *(emphasis added)*

Applicants submit that these sections more than sufficiently clarify the limitation "misprediction value". The Examiner's arguments seem to require all of the sections describing the limitation "misprediction value" to be literally present in the claims. Clearly, this is contrary to the applicable law. Claims are meant to be read in light of the specification, and when done so in this case, the term "misprediction value" is clear. As such, the Examiner's claims that "[n]one of this language is recited within the claims" is moot and inapplicable. *See* Examiner's Answer, page 22.

In order to support a proper §103(a) rejection, the cited must show a "misprediction value," which is described the claims(*see* e.g., claim 1). As argued previously, using a misprediction value to determine whether to reverse a branch prediction is not found in the cited references. In fact, the cited references do not describe *the reversing a branch prediction at all.* As such, the cited references are inapplicable and insufficient to support a proper rejection.

C. Applicants' reply to Examiner's assertion regarding a) pages10-11 and 12-13 and b) pages 12 of the Appeal Brief. *See* Examiner's Answer, pages 22-26.

As argued above, claims are read in light of the specification. Therefore, when evaluating the limitation "base misprediction history register", the specification must be considered when evaluating the claims in view of the prior art. As stated previously, clarification of the meaning of the term may be found at page 6, lines 16-20 of the specification, which state:

> As discussed above, base misprediction history register 110 reflects the correctness of the base predictor standing alone. Unlike global history registers that record whether previous branches were taken or not taken, base misprediction history register 110 records whether previous branch predictions were correctly predicted by the base predictor.

Other examples may be found at page 9, lines 9-10 and page 8, lines 2-3. Therefore, in light of the arguments made above (pertaining to the relationship of claims to the specification), Applicants submit the Examiner's claims that "[n]one of this language is recited within the claims" is moot and inapplicable. *See* Examiner's Answer, page 26. In addition, Applicants reiterate that their arguments made in the Appeal Brief that none of the cited sections describe such a limitation.

The Examiner also erroneously claims Tran has taught two elements which could be considered a "base misprediction history register" as described in embodiments of the present application (e.g., *see* claims 1, 24). *See* Examiner's Answer, pages 23-24 (and again citing the same sections on pages 24-25). In describing the first element, she cites column 13, lines 17-35; column 14, lines 36-38; and column 14 lines 42-54 of Tran.

Column 13, lines 17-35 state:

> Branch tags register 50 initially stores a set of branch tags "0" through "F" in the embodiment shown in FIG. 3. Therefore, up to sixteen branch instructions may be concurrently outstanding within the instruction processing pipeline of microprocessor 10. Branch tag "0" is the first tag to be assigned, followed by branch tag "1", etc. As branch tags are assigned from the head of branch tags shift register 50, the tags are rotated to the tail of branch tags shift register 50. Additionally, the tail of storage 56 stores the branch prediction information associated with the branch instruction being predicted when the shift signal is asserted. As additional branch instructions are predicted, the branch tags within branch tags shift register 50 are rotated. *The corresponding branch prediction information is shifted within storage 56 such that the branch prediction information remains stored in a storage location within storage 56 which corresponds to the storage location within branch tags shift register 50 in which the branch tag is stored. (emphasis added)*

The cited section discusses the use of sixteen "branch tags". It further states that the cited branch tags shift register assigns the branch tags, and the tail of storage stores "branch prediction information". However, "branch prediction information" is not the same as a "branch

misprediction history". The cited section is dedicated toward providing proper branch prediction (*see* emphasis). There is no mention of monitoring *misprediction* information whatsoever, and even more so, no mention of a *register specifically dedicated to recoding the history of mispredictions.*

Next, column 14, lines 36-38 state:

> The comparator compares the branch tag within that storage location to the mispredicted branch tag conveyed upon mispredicted branch tag bus 72.

Contrary to the Examiner's assertion, this section does not pertain to the branch tags shift register 50 at all. In addition, although the cited section describes a "mispredicted branch tag", it does not describe a *register specifically dedicated to recording the history of mispredictions.*

Next, Column 14, lines 42-54 states:

> Because the branch instruction is mispredicted, branch instructions fetched subsequent to the mispredicted branch instruction lie within an incorrectly predicted instruction stream. These branch instructions are discarded by reorder buffer 32 upon detection of the mispredicted branch, and likewise should be discarded from storage 56. Therefore, control unit 54 resets the valid bits corresponding to branch instructions which are subsequent to the mispredicted branch instruction to the invalid state. Since storage 56 and branch tags register 50 are implemented as shift registers in the present embodiment, those valid bits between the tail of storage 56 and the location identified by comparator block 52 are reset.

The cited section describes the discarding of branch instructions in a pipeline once a branch instruction is mispredicted. Once the misprediction occurs, the valid bits of storage 56 are reset. Applicants submit this section does not describe generating a misprediction history, nor does not describe a register dedicated to that purpose. Therefore, contrary to the Examiner's assertion that the branch tags register 50 is the same as a branch misprediction history register is simply erroneous.

For at least the following reasons, the second cited element fails to describe the relevant limitations as well. The second cited alleged equivalent is allegedly described in column 13 lines 50-59, column 15, lines 48-54 and column 14, lines 55-65. Column 13, lines 50-59 state:

> Valid shift register 60 stores a valid indication for each branch instruction. If the valid indication is in a valid state, then the corresponding taken/not-taken prediction and branch prediction information is valid (i.e. *corresponds to a branch instruction which is outstanding within the instruction processing pipeline of microprocessor 10*). Alternatively, if the valid indication is in the invalid state then the corresponding taken/not-taken prediction and branch prediction information is invalid (i.e. *does not correspond to a branch instruction which is outstanding within the instruction processing pipeline of microprocessor 10*). (*emphasis added)*

Applicants submit that the valid shift register 60 is not directed to mispredictions at all, but instead to whether a branch is "outstanding", i.e., whether it is yet to be executed. Whether a instruction is yet to be executed has no relationship to whether a instruction has been mispredicted. The cited section does not pertain to a branch misprediction history register at all.

Next, the Examiner cites column 15, lines 48-54, which state:

> When the valid bit at the head of valid shift register 60 indicates invalid (through branch misprediction or retirement of a branch instruction), the stall signal is deasserted and instruction fetch continues.
>
> In another embodiment, a branch tag is assigned to each cache line of instructions as the instructions are fetched from instruction cache 16.

This section describes the operation of valid shift register 60 when a valid bit indicates invalid (e.g., a misprediction). A stall signal is de-asserted and the instruction fetch continues. Although the cited section describes misprediction as one of the criteria for an "invalid", there is no mention of *generating a misprediction history* or *register specifically dedicated to recoding the history of mispredictions*.

Lastly, column 14, lines 55-65 state:

> In addition to resetting the valid bits as described above, control unit 54 adjusts branch tags shift register 50 and storage 56 in response to a mispredicted branch instruction. In particular, control unit 54 rotates the branch tags such that the branch tag subsequent to the mispredicted branch tag is at head of branch tags shift register 50. Storage 56 is adjusted accordingly, such that the branch prediction information corresponding to each branch tag is in a storage location within storage 56 which is associated with the storage location within branch tags shift register 50 storing that branch tag.

The cited section describes the operation of branch tags shift register 50 and storage 56 in response to a mispredicted branch instruction. A control unit 54 adjusts the sequence of the branch tags, including the branch tag associated with the misprediction. A corresponding adjustment is made to storage 56 such that the branch prediction information for each branch tag pertaining to future predictions matches up with storage location within storage 56, thereby allowing the different components system to adjust to the misprediction and continue to operate.

Applicants submit that this section does not pertain to misprediction *history, recording misprediction history, or a register specifically dedicated to recoding the history of mispredictions* at all. Furthermore, Applicants submit, as shown above, none of these sections cited by the Examiner, describe a *base misprediction history register* as specifically described in embodiments of present application.

D. Applicants' reply to Examiner's assertions regarding claim 27 in Examiner's Answer. *See* Examiner's Answer dated 1/21/2006, pages 11-12.

The Examiner concedes Tran does not teach flushing an instruction pipeline processing said branch instruction. It asserts Applicants Admitted Prior Art ("AAPA") has taught flushing an instruction pipeline processing said branch instruction. *See* id. Applicants respectfully disagree and also maintain, as argued in the Appeal Brief, that both the AAPA and the Tran

reference fails to teach at least a "base misprediction history register" as described in the embodiment of claim 24. As such, Applicants submit claim 24 and claim 27 (depending from claim 24) are allowable in their present form.

CONCLUSION

In view of the above, Appellant respectfully submits that the rejection of claims 1-8, 10-15, 17-23 and 24-26 should be reversed. Appellant therefore respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting claims 1-8, 10-15, 17-23 and 24-26 and direct the Examiner to pass the case to issue.

The Examiner is hereby authorized to charge any additional fees which may be necessary for consideration of this paper to Kenyon & Kenyon LLP Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON LLP

Date: January 22, 2007

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